Patent Application
Docket No. UF-318X
Serial No. 10/613,963

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Examiner	:	Sai Ming Chan
Art Unit	:	2616
Applicant(s)	:	Sahni *et al.*
Serial No.	:	10/613,963
Conf. No.	:	6767
Filed	:	July 3, 2003
For	:	Dynamic IP Router Using Highest Priority Matching

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

DECLARATION OF SARTAJ KUMAR SAHNI, PH.D., UNDER 37 CFR 1.132

Sir:

I, Sartaj Kumar Sahni, declare as follows:

1. I am a co-inventor of the above-identified U.S. patent application.

2. I have extensive experience in this field as evidenced by my attached *curriculum vitae*. *See Exhibit A.*

3. I am familiar with the technology described and claimed in the above-identified U.S. patent application;

4. I have reviewed and am familiar with Application Serial No. 10,613,963; the claims currently pending therein; the Office Action dated May 13, 2008; the Yazdani *et al.* ("Yazdani" U.S. Patent No. 6,859,455) and Rajasekaran *et al.* ("Rajasekaran" U.S. Pat. Pub. No. 2002/0124003) references cited therein, and the Turner *et al.* (U.S. Patent No. 6,018,524) reference cited in the Office Action dated March 19, 2007.

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5. The Yazdani patent covers 3 data structures—a balanced binary search tree, a static m-way search tree, and a dynamic m-way search tree—for packet routing. The balanced binary search tree is obtained by sorting the prefixes and setting up a binary search tree for these prefixes to mirror a binary search. This is further explained in the textbook "Fundamentals of Data Structures" (Computer Science Press, Maryland, 1976) written by me, Sartaj Sahni and Ellis Horowitz, and in the textbook "Fundamentals of Data Structures in C++" (W.H. Freeman, NY, 1995) written by me, Sartaj Sahni, and Ellis Horowitz and Dinesh Mehta.

6. Referring to the Yazdani patent, the binary search tree of Figure 4 is given as an example of a search that fails to find the longest matching prefix (see col. 15, lines 3-14). The binary search tree shown in Figure 4 is not a balanced binary search tree (PTST). Rather, each node of the binary search tree shown in Figure 4 stores a prefix and not a point value as specified by the claims.

7. The term "level" is used in Yazdani *et al.* to refer to the distance from the tree root, i.e., the tree root is at level 0, its children are at level 1, their children at level 2, and so forth. In contrast, the claimed top level balanced binary search tree (PTST) has at least one node comprising a lower level range search tree (RST). This context refers to an embedding level. The entire tree constructed by each of Yazdani's methods is a top-level tree. None of the trees disclosed by Yazdani include lower-level embedded trees or other embedded structures.

8. Although the balanced binary search tree used by Yazdani can be searched for the longest matching prefix in O(log n) time, where n is the number of prefixes, it is impossible to insert or delete into/from this structure in less than linear (O(n)) time. This is because a single insert/delete can change the entire sequence of medians used to construct the tree in the first place (column 16, lines 37-56, Yazdani). Two insert procedures are described in column 18, lines 43-67 and column 19, lines 1-29 of Yazdani. Neither attempts to maintain a balanced search tree. As a result, following a series of inserts, the tree height becomes O(n) (see Sahni's data structure texts for worst-case performance of inserts/deletes that do not maintain balance) and all operations search/insert/delete run in O(n) time. The static m-way structure patented by Yazdani is a generalization of their binary tree structure and suffers from the same deficiencies as far as insert/delete are concerned. The

dynamic m-way structure uses a standard B-tree (B-trees were invented in 1972, see Sahni's data structure text for a description). However, for Yazdani's stated application, it is necessary to sort elements in subtrees and relocate them (column 21, lines 4-5). This makes the insert process inefficient. Further, no process is described to delete a prefix. As stated earlier, it is impossible to insert/delete from the Yazdani structures in O(log n) time.

9. The structure of Turner has an expected (not worst case) search complexity of O(log W), where W is the length of the longest prefix (more accurately, W may be replaced by the number of different prefix lengths). The worst-case search complexity is O(logW * log n) (provided sets of hash synonyms are maintained as balanced search trees) and so is inferior, in the worst-case, to that of Yazdani. The insert/delete complexity is $O(n \log^2 W)$ and because of the need to keep markers in each of the hash tables, it is impossible to insert/delete in O(log n) or O(log W) time using this structure.

10. As indicated above, it is impossible to get efficient insert/delete complexities using the structures of Yazdani or Turner or a combination thereof.

11. Even if it were possible to develop efficient balancing methods for the structures of Yazdani and Turner, the resulting balanced structures would be fundamentally different from those in the present patent application. For example, the Yazdani structures are single-level structures while those of the present patent are two-level structures and balancing methods do not change the number of levels (in the sense of number of levels of embedding).

12. The binary-tree on binary-tree (BOB) data structure of certain claimed embodiments in the current patent application employs red-black search trees (a popular variety of balanced binary search tree) in a very unique manner. Unlike Yazdani's search tree (which is not a red-black tree but one derived by mimicking a binary search on a sorted list), we use a binary search tree (e.g., a red-black tree) of points at the top level. Each node of this top-level red-black tree contains another red-black tree, which contains a subset of the ranges/prefixes in the router table. The total number of binary search trees in our data structure is equal to the number of node in the top-level tree plus 1. Note that Yazdani stores a single prefix in each node of a binary search tree; we store several

prefixes in each node of the top-level tree together with a single point.

13. The two data structures are very different—Yazdani is a traditional binary-search based binary search tree of prefixes, ours can be a red-black tree in which each node is itself a red-black tree.

14. To obtain the $O(\log^2 n)$ search and $O(\log n)$ insert/delete complexities claimed by us, we had to invent the idea of retaining a limited number of empty nodes in the structure (something that is not done in any other dynamic structure we are aware of). We were able to prove that even with the empty nodes counted, at most 2n nodes are needed in the red-black tree to enable the claimed complexities. Without these empty nodes, it isn't possible to get the claimed complexities.

15. Furthermore, our structure can do packet routing efficiently under any one of the following conditions—the highest priority matching prefix is to be used, the longest matching prefix is to be used, the rules are nonintersecting ranges with priority. The structures proposed in the Yazdani and Turner patents can be used only to find the longest matching prefix and cannot be extended for the other two conditions. As noted above, neither supports efficient insert/delete as supported by our structure.

16. The teachings of Rajasekaran have no relationship to our work or that of Yazdani. While Rajasekaran cite some prior art for balanced search tree structures for exact match, this prior art does not apply in any rational way to prefix matching (longest or highest priority) or to range matching and they do not attempt to address this problem.

17. Although Rajasekaran use arrays of pointers, null pointers and arrays of bits, these are standard data structure concepts with wide applicability (see any data structures book). They do not use ALLs (array linear lists, which are not the same as arrays). The bit arrays used by them are to keep track of null and non-null pointers. The claimed ALLs and bit vectors are used for entirely different purposes than the pointer and bit arrays of Rajasekaran.

18. I hereby further declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are

punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

By: ________________________ July 16, 2008
Date

SAATAJ SAHNI

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EXHIBIT A

Dr. Sartaj Sahni

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LINKS

1. Wikipedia.
2. Mathematics Genealogy Project.

AREAS OF SPECIALIZATION

1. Sequential and parallel data structures and algorithms.
2. Scheduling.
3. Optimization.
4. VLSI CAD.
5. Computational geometry.
6. Image processing.
7. Medical applications.

EDUCATIONAL BACKGROUND

1. Ph.D., Computer Science, Cornell University, 1973.
2. M.S., Computer Science, Cornell University, 1972.
3. B.Tech. (Electrical Engineering), Indian Institute of Technology, Kanpur, 1970.

EMPLOYMENT

2001 - Present	Chair, CISE, University of Florida
1998 - Present	Distinguished Professor, CISE, University of Florida
1990 - 1998	Professor, CISE, University of Florida
1981 - 1990	Professor, Computer Science, University of Minnesota
1977 - 1981	Associate Professor, Computer Science, University of Minnesota
1973 - 1977	Assistant Professor, Computer Science, University of Minnesota

Ph.D. STUDENTS

1. Teofilo Gonzalez, 1975
2. Yookun Cho, 1978
3. David Nassimi, 1979
4. Eliezer Dekel, 1981
5. Raghunath Raghavan, 1982
6. Jim Cohoon, 1982

7. Ten-Hwang Lai, 1982
8. Rajiv Kane, 1984
9. Sangyong Han, 1984
10. Kam-Hoi Cheng, 1985
11. Jayaram Bhasker, 1985
12. Lishin Lin, 1986
13. Surendra Nahar, 1986
14. Jong Lee, 1987
15. Youngju Won, 1987
16. Sanjay Ranka, 1988
17. Jin Woon Woo, 1989
18. Wing Ning Li, 1989
19. San Yuan Wu, 1989
20. Patrick Jarvis, 1990
21. Jing-Fu Jenq, 1990
22. Kyunrak Chong, 1991
23. Doowon Paik, 1991
24. Mario Lopez, 1991
25. Andrew Lim, 1992
26. Keumog Ahn, 1992
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28. Madhusudan Nigam, 1992
29. Venkat Thanvantri, 1995
30. Seonghun Cho, 1996
31. Chih-Fang Wang, 1998
32. Edward Cheng, 1998
33. Haejae Jung, 2000
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35. Kun Suk Kim, 2003
36. Meongchul Song, 2005
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38. Joonseok Park, 2005
39. Kevin McCullen, 2006
40. Wencheng Lu, 2007
41. Xiaochun Xu, 2008

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BOOKS/PROCEEDINGS, EDITED

1. Sartaj Sahni, *Proceedings 1987 International Conference on Parallel Processing*, Pennsylvania State University Press, PA, 1987, 993 pages.
2. Sartaj Sahni, Viktor Prasanna, and Vijay Bhatkar, *High Performance Computing*, Proceedings of the International Conference on High Performance Computing, New Delhi, India, Tata McGraw Hill, 1995, 788 pages.
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2. Area Editor, Algorithms for Multiprocessors, *Jr of Parallel & Distributed Computing*, 1986-92.
3. Member, Editorial Advisory Board, *Information & Software Technology*, Butterworth Scientific Ltd. 1986-1994.
4. Member, Editorial Advisory Board, *Computer Systems: Science and Engineering*, Butterworth Scientific Ltd. 1988-.
5. Associate Editor, *IEEE Transactions on Parallel and Distributed Systems*. 1991-1994.

6. Co-Editor, Theory, Algorithms, and Programming, *Jr of Parallel & Distributed Computing*, 1992-.
7. Co-Editor, *Parallel Computing Series*, Chapman-Hall, England, 1992-1994.
8. Associate Editor, *IEEE Parallel and Distributed Technology: Systems and Applications*, 1992-96.
9. Associate Editor, *IEEE Concurrency*, 1996-97.
10. Member, Editorial Board, *International Journal of Foundations of Computer Science*, 1997-1999.
11. Managing Editor, *International Journal of Foundations of Computer Science*, 1999-.
12. Member, Editorial Board, *Parallel Processing Letters*, 2001-.
13. Editor-in-Chief, *Computer and Information Science Series*, Chapman & Hall/CRC, 2002-.
14. Member, Editorial Board, *International Journal of Computational Science and Engineering*, 2003-.
15. Member, Editorial Board, *International Journal of High Performance Computing and Networking*, 2004-.
16. Member, Editorial Board, *International Journal of Distributed Sensor Networks*, 2004-.
17. Member, Advisory Board, *International Journal of Pervasive Computing and Communications*, 2004-.
18. Member, International Advisory Board, *Sultan Qaboos University Journal for Science*, 2005-.
19. Member, Editorial Advisory Board, *Enterprise Information Systems*, Taylor and Francis. 2006-.
20. Member, Editorial Board, *Lecture Notes on ICST Activities* (Institue for Computer Sciences, Social-Informatics, and Telecommunications Engineering), Springer Verlag, 2008-.

PROFESSIONAL ACTIVITIES

1. Member, Conference advisory committee, Foundations of software technology and theoretical computer science, India, 1980-1990.
2. Chairman, Computer Science Curriculum, National Technological University, Colorado, 1983-.
3. Member, Advisory Board, Bilkent University, Ankara, Turkey, 1987.
4. Program Chair, 1987 IEEE International Conference on Parallel Processing.
5. General Chair, 1991 IEEE Symposium on Parallel and Distributed Processing.
6. Steering Committee Member, IEEE Symposium on Parallel and Distributed Processing (SPDP), 1991 and 1995.
7. Steering Committee Member, International Conference on High Performance Computing (HiPC), 1995-.
8. Member, Steering Committee, International Parallel Processing Symposium (IPPS) (renamed IPDPS in 1999), 1996-.
9. Member, Advisory Committee, International Symposium on Parallel Architectures, Algorithms and Networks, 1997-.

10. Member, Advisory Committee, Workshop on Randomization Methods in Algorithm Design, 1997-.
11. Member, Steering Committee, Workshop on Biologically Inspired Solutions to Parallel Processing Problems (BioSP3), 1997-.
12. Keynote Speaker, Second Great Lakes Computer Science Conference, Western Michigan University, Kalamazoo, Oct. 17, 1991.
13. Keynote Speaker, 5th Workshop on Algorithmic Research in the Midsouth, Southwest Louisiana University, Lafayette, April 24, 1992.
14. Member, Advisory Committee, IEEE Technical Committee on Parallel Processing, 1993-96.
15. Chair, IEEE Technical Committee on Parallel Processing, 1996-1999.
16. Vice Chair, IEEE Technical Committee on Parallel Processing, 1999-.
17. Program Vice-chair for algorithms and applications, 8th International Parallel Processing Symposium, 1994.
18. Program Chair, Systems Track, IEEE Symposium on Parallel and Distributed Processing, 1995.
19. Keynote Speaker, International Parallel Processing Symposium, 1995.
20. Program Chair, International Conference on High Performance Computing, 1995-1997.
21. Program Vice-chair for algorithms, International Parallel Processing Symposium, 1997.
22. Program Chair, International Parallel Processing Symposium, 1998.
23. Keynote Speaker, International Symposium on Parallel Architectures, Algorithms, and Networks, 1999.
24. Keynote Speaker, IEEE International High Performance Computing Conference, 1999.
25. Poster/presentation Chair, IEEE International Conference on High Performance Computing, 1999-2001.
26. Keynote Speaker, Hawaiian International Conference on System Sciences, 2000.
27. Member, Steering committee, Workshop on Advances in Parallel and Distributed Computational Models, 2000-.
28. General Chair, Seventh International Workshop on Solving Irregularly Structured Problems in Parallel, 2000.
29. Program Co-chair, 7th IEEE International Conference on Parallel Interconnect, 2000.
30. Member, Advisory Committee, Emerging Technology Track, Hawiian International Conference on System Sciences (HICSS34), 2001.
31. Keynote speaker, Workshop on Advances in Parallel and Distributed Computational Models, 2001.
32. Steering Committee Member, 13th International Conference on Parallel and Distributed Computing and Systems (PDCS), 2001.
33. Program Vice-chair for algorithms, International Symposium on Parallel Architectures, Algorithms, and Networks, 2002.
34. Advisory Committee Member, 14th International Conference on Parallel and Distributed Computing and Systems (PDCS), 2002.

35. Chair, Search Committee for Editor-in-Chief of IEEE Transactions on Computers, 2002.
36. Keynote speaker, Eighth International Conference, COCOON, 2002.
37. Keynote speaker, International Symposium on Parallel Architectures, Algorithms, and Networks, 2002.
38. Program Committee Chair, IEEE International High Performance Computing Conference, 2002.
39. Member, Advisory Committee, Software Track, Hawiian International Conference on System Sciences (HICSS36), 2003.
40. Publications Chair, IEEE Symposium on Applications and the Internet, SAINT, 2003.
41. Conference Chair, IASTED Conference on Computer Science and Technology, CST 2003-.
42. Keynote speaker, IEEE International Symposium on Computers and Communications, ISCC, 2003.
43. Keynote speaker, International Conference on Advanced Computing and Communications, ADCOM, 2003.
44. Member, Advisory Board, Labortory for Interdisciplinary Information Science and Technology, University of Central Florida, 2005-.
45. Keynote speaker, International Symposium on Parallel and Distributed Processing and Aplications, ISPA, 2005.
46. Co-chair, Steering Committee, International Symposium on Parallel and Distributed Processing and Aplications, ISPA, 2005.
47. Member, Advisory Board, International Conference on Innovations and Real-Time Applications of Distributed Sensor Networks, 2005-.
48. Co-Conference Chair, International Conference on Information Technology, Systems and Management.
49. Keynote Speaker, IEEE Sensor Networks, Ubiquitous, and Trustworthy Computing, 2006.
50. Steering Committee Member, IEEE International Conference on Computers and Communication, 2007-.
51. Conference co-chair, International Conference on Information Systems, Management and Technology, 2007-.
52. R. C. Bose Memorial Keynote Speaker, International Conference on Interdisciplinary Mathematical and Statistical Techniques, Shanghai, China, 2007.
53. Member, Advisory Board, International Conference on Technology, Communication and Education, IEEE, 2008.
54. Keynote Speaker, International Conference on Information Systems, Technology, and Management, Dubai, UAE, 2008.
55. Keynote Speaker, International Symposium on Advances in Computer and Sensor Networks, Zhengzhou, China, 2008.
56. Distinguished Lecture Series speaker at several universities.
57. External reviewer for several CS and CSE departments in the US and international.
58. Served on several NSF and NIH panels.
59. Served as session chair at several conferences.

60. Member of many conference program committees.
61. Reviewed papers for numerous journals and conferences.
62. Have given many invited presentations at national and international conferences and at universities and industrial organizations.

HONORS AND AWARDS

1. Colonel Ogilive medal 1965, First in All India Higher Secondary Exam (several thousand students).
2. Science Talent Search Scholarship, 1965.
3. President of India Gold Medal, First in class 1970, IIT/Kanpur, May 1970 (approx. 300 students).
4. Silver Medal, First in Electrical Engineering, IIT/Kanpur, May 1970 (approx. 80 students).
5. IBM Fellowship, Cornell University, 1970-1971.
6. Cornell University Fellowship, 1971-1973.
7. IEEE certificate of appreciation, 1982.
8. Outstanding Professor Award, Institute of Technology Student Board, University of Minnesota, 1986.
9. Senior Member, IEEE, August 1986.
10. Distinguished service award, International Conference on Parallel Processing, 1987.
11. Certificate of appreciation, 1987 Conference on expert systems technology in the ADP environment.
12. Fellow, Supercomputer Institute, University of Minnesota, 1985.
13. Fellow, IEEE, Jan. 1988. Citation: For contributions to computer algorithms, computer-aided design, and large-scale systems.
14. University of Minnesota Rochester Center for Continuing Education and Extension certificate for ``outstanding service and dedication in teaching", 1989.
15. Research achievement award, University of Florida, 1992.
16. IEEE meritorious service certificate, 1995.
17. Fellow, American Association for the Advancement of Science (AAAS), Oct. 1995. Citation: For contributions to the design and analysis of algorithms, parallel computing, and electronic computer aided design.
18. Teaching Incentive Program Award, University of Florida, 1995.
19. Fellow, Association for Computing Machinery (ACM), 1996. Citation: For contributions to data structures, design and analysis of algorithms, multiprocessor scheduling, electronic computer-aided design, and parallel computing.
20. Charter Member, IEEE Computer Society's Golden Core, 1996.
21. IEEE Computer Society Taylor L. Booth Education Award ``for contributions to Computer Science and Engineering education in the areas of data structures, algorithms, and parallel algorithms", 1997.
22. University of Florida Research Foundation Professorship, 1997-2000.
23. Distinguished Alumnus Award, Indian Institute of Technology, Kanpur, ``in recognition of his outstanding and seminal contributions in the field of Computer Science and Engineering", 2001.
24. Original Member, Highly Cited Researchers Database, 2002.

25. Member, European Academy of Sciences, 2002. Citation: For outstanding and lasting contributions to computer science and fundamental developments in the area of data structures and algorithms.
26. ACM recognition of service award, 2002.
27. IEEE Computer Society W. Wallace-McDowell Award, 2003. Citation: For contributions to the theory of NP-hard and NP-complete problems.
28. ACM Karl Karlstrom Outstanding Educator Award, 2003. Citation: For outstanding contributions to computing education through inspired teaching, development of courses and curricula for distance education, contributions to professional societies, and authoring significant textbooks in several areas including discrete mathematics, data structures, algorithms, and parallel and distributed computing.
29. *Best Paper Award*. X. Xu and S. Sahni, Approximation algorithms for sensor deployment. *Innovations and Real-Time Applications of Distributed Sensor Network (DSN) Symposium*, 2006.
30. *Best Paper Award*. S. Sahni, N. Rao, S. Ranka, Y. Li, E. Jung, and N. Kamath, Bandwidth scheduling and path computation algorithms for connection-oriented networks. *International Conference on Networking*, 2007.

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The remaining sections of this chapter are organized around different ways to implement symbol tables. Different strategies are preferable given different assumptions. The first case considered is where the identifiers are known in advance and no deletions or insertions are allowed. Symbol tables with this property are called *static*. One solution is to sort the names and store them sequentially. Using either the binary search or Fibonacci search method of section 7.1 allows us to find any name in $O(\log_2 n)$ operations. If each name is to be searched for with equal probability then this solution, using an essentially balanced binary search tree, is optimal. When different identifiers are searched for with differing probabilities and these probabilities are known in advance this solution may not be the best. An elegant solution to this problem is given in section 9.1.

In section 9.2 we consider the use of binary trees when the identifiers are not known in advance. Sequential allocation is no longer desirable because of the need to insert new elements. The solution which is examined is AVL or height balanced trees. Finally in section 9.3 we examine the most practical of the techniques for dynamic search and insertion, hashing.

9.1 STATIC TREE TABLES

Definition: A *binary search tree T* is a binary tree; either it is empty or each node in the tree contains an identifier and:

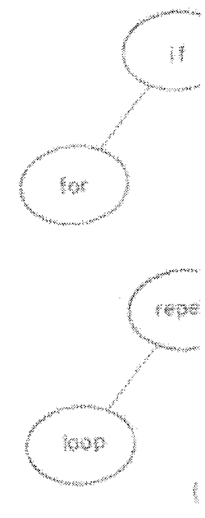
(i) all identifiers in the left subtree of T are less (numerically or alphabetically) than the identifier in the root node T;

(ii) all identifiers in the right subtree of T are greater than the identifier in the root node T;

(iii) the left and right subtrees of T are also binary search trees. For a given set of identifiers several binary search trees are possible. Figure 9.1 shows two possible binary search trees for a subset of the reserved words of SPARKS.

To determine whether an identifier X is present in a binary search tree, X is compared with the root. If X is less than the identifier in the root, then the search continues in the left subtree; if X equals the identifier in the root, the search terminates successfully; otherwise the search continues in the right subtree. This is formalized in algorithm SEARCH.

From Fundamentals of Data Structures by Horowitz and Sahni; Computer Science Press, 1976




```
procedure S
  //search
  LCHIL
  Otherw
  binary
  i ← T
  while i ≠
    case
      :X < I
      :X = I
      :X > I
    end
  end
end SEAR
```

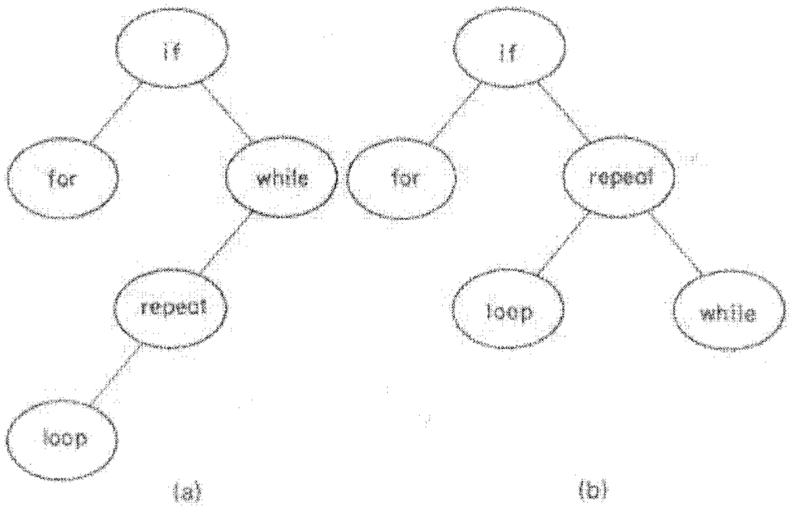


Figure 9.1 Two possible binary search trees

```
procedure SEARCH(T,X,i)
  //search the binary search tree T for X. Each node has fields
    LCHILD, IDENT, RCHILD. Return i = 0 if X is not in T.
    Otherwise, return i such that IDENT(i) = X. LCHILD(empty
    binary tree) = RCHILD(empty binary tree) = 0.//
  i ← T
  while i ≠ 0 do
    case
      :X < IDENT(i): i ← LCHILD(i)        //search left subtree//
      :X = IDENT(i): return
      :X > IDENT(i): i ← RCHILD(i)        //search right subtree//
    end
  end
end SEARCH
```

In our study of binary search in chapter 7, we saw that every sorted file corresponded to a binary search tree. For instance, a binary search on the file (**do**, **if**, **stop**) corresponds to using algorithm SEARCH on the binary search tree of figure 9.2. While this tree is a full binary tree, it need not be optimal over all binary search trees for this file when the identifiers are searched for with different probabilities. In order to determine an optimal binary search tree for a given static file,

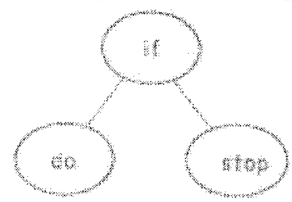


Figure 9.2 Binary search tree corresponding to a binary search on the file (**do**,**if**,**stop**).

we must first decide on a cost measure for search trees. In searching for an identifier at level k using algorithm SEARCH, k iterations of the **while** loop of lines 2–8 are made. Since this loop determines the cost of the search, it is reasonable to use the level number of a node as its cost.

Consider the two search trees of figure 9.1 as possibly representing the symbol table of the SPARKS compiler. As names are encountered a match is searched for in the tree. The second binary tree requires at most three comparisons to decide whether there is a match. The first binary tree may require four comparisons, since any identifier which alphabetically comes after **if** but precedes **repeat** will test four nodes. Thus, as far as worst case search time is concerned, this makes the

balanced binary search tree that mimics a binary search

while the table is being built and so it is difficult to achieve this ideal without making the time required to add new entries very high. This is so because in some cases it would be necessary to restructure the whole tree to accommodate the new entry and at the same time have a full binary search tree. It is, however, possible to keep the trees balanced so as to ensure both an average and worst case retrieval time of $O(\log n)$ for a tree with n nodes. We shall study one method of growing balanced binary trees. These balanced trees will have satisfactory search and insertion time properties.

Height Balanced Binary Trees

Adelson-Velskii and Landis in 1962 introduced a binary tree structure that is balanced with respect to the heights of subtrees. As a result of the balanced nature of this type of tree, dynamic retrievals can be performed in $O(\log n)$ time if the tree has n nodes in it. At the same time a new identifier can be entered or deleted from such a tree in time $O(\log n)$. The resulting tree remains height balanced. The tree structure introduced by them is given the name AVL-tree. As with binary trees it is natural to define AVL trees recursively.

Definition: An empty tree is height balanced. If T is a nonempty binary tree with T_L and T_R as its left and right subtrees, then T is *height balanced* iff (i) T_L and T_R are height balanced and (ii) $|h_L - h_R| \leq 1$ where h_L and h_R are the heights of T_L and T_R respectively.

The definition of a height balanced binary tree requires that every subtree also be height balanced. The binary tree of figure 9.7 is not height balanced since the height of the left subtree of the tree with root 'APRIL' is 0 while that of the right subtree is 2. The tree of figure 9.8 is height balanced while that of figure 9.9 is not. To illustrate the processes involved in maintaining a height balanced binary search tree, let us try to construct such a tree for the months of the year. This time let us assume that the insertions are made in the order MARCH, MAY, NOVEMBER, AUGUST, APRIL, JANUARY, DECEMBER, JULY, FEBRUARY, JUNE, OCTOBER and SEPTEMBER. Figure 9.10 shows the tree as it grows and the restructuring involved in keeping the tree balanced. The numbers within each node represent the difference in heights between the left and right subtrees of that node. This number is referred to as the balance factor of the node.

Definition: The *balance factor*, $BF(T)$, of a node T in a binary tree is defined to be $h_L - h_R$ where h_L and h_R are the heights of the left

Loading Order

As in the case of internal tables, the order in which key values are entered into the hash table is important. To the extent possible, an attempt should be made to enter these values in order of nonincreasing frequency of search. When this is done, new entries should be added to the end of the overflow chain rather than at the front.

10.2.3 Tree Indexing—*B*-Trees

The AVL tree of §9.2 provided a means to search, insert and delete entries from a table of size n using at most $O(\log n)$ time. Since these same functions are to be carried out in an index, one could conceivably use AVL trees for this application too. The AVL tree would itself reside on a disk. If nodes are retrieved from the disk, one at a time, then a search of an index with n entries would require at most 1.4 log n disk accesses (the maximum depth of an AVL tree is 1.4 log n). For an index with a million entries, this would mean about 23 accesses in the worst case. This is a lot worse than the cylinder sector index scheme of §10.2.1. In fact, we can do much better than 23 accesses by using a balanced tree based upon an m-way search tree rather than one based on a binary search tree (AVL trees are balanced binary search trees).

Definition: An *m-way search tree*, T, is a tree in which all nodes are of degree $\leq m$. If T is empty, (i.e., $T = 0$) then T is an m-way search tree. When T is not empty it has the following properties:

(i) T is a node of the type

$$n, A_0, (K_1, A_1), (K_2, A_2), \ldots, (K_n, A_n)$$

where the A_i, $0 \leq i \leq n$ are pointers to the subtrees of T and the K_i, $1 \leq i \leq n$ are key values.

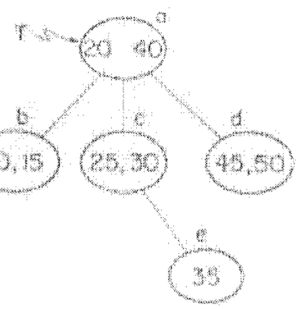
(ii) $K_i < K_{i+1}$, $1 \leq i < n$

(iii) All key values in the subtree A_i are less than the key value K_{i+1}, $0 \leq i < n$

(iv) All key values in the subtree A_n are greater than K_n.

(v) The subtrees A_i, $0 \leq i \leq n$ are also m-way search trees.

As an example of a 3-way search tree consider the tree of figure 10.9 for key values 10, 15, 20, 25, 30, 35, 40, 45 and 50. One may easily verify that it satisfies all the requirements of a 3-way search



node	schematic format
a	2,b,(20,c),(40,d)
b	2,0,(10,0),(15,0)
c	2,0,(25,0),(30,e)
d	2,0,(45,0),(50,0)
e	1,0,(35,0)

Figure 10.9 Example of a 3-way search tree.

tree. In order to search for any key value X in this tree, we first "look into" the root node $T = a$ and determine the value of i for which $K_i \le X < K_{i+1}$ (for convenience we use $K_0 = [-\infty]$ and $K_{n+1} = [+\infty]$ where $[-\infty]$ is smaller than all legal key values and $[+\infty]$ is larger than all legal key values). In case $X = K_i$ then the search is complete. If $X \ne K_i$ then by the definition of an m-way search tree X must be in subtree A_i if it is in the tree. When n (the number of keys in a node) is "large," the search for the appropriate value of i above may be carried out using binary search. For "small" n a sequential search is more appropriate. In the example if $X = 35$ then a search in the root node indicates that the appropriate subtree to be searched is the one with root $A_1 = c$. A search of this root node indicates that the next node to search is e. The key value 35 is found in this node and the search terminates. If this search tree resides on a disk then the search for $X = 35$ would require accessing the nodes a, c and e for a total of 3 disk accesses. This is the maximum number of accesses needed for a search in the tree of figure 10.9. The best binary search tree for this set of key values requires 4 disk accesses in the worst case. One such binary tree is shown in figure 10.10.

Algorithm MSEARCH searches an m-way search tree T for key value X using the scheme described above. In practice, when the search tree

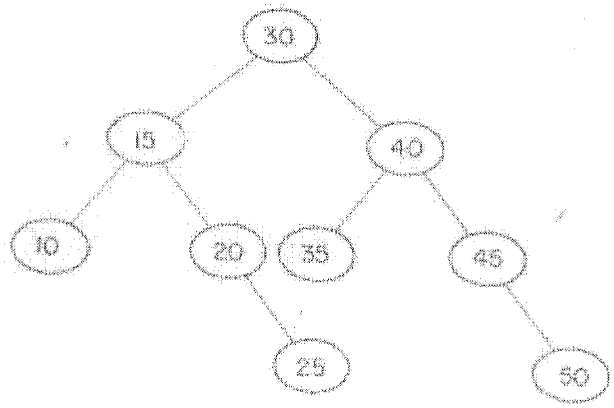


Figure 10.10 Best AVL-tree for data of figure 10.9

represents an index, the tuples (K_i, A_i) in each of the nodes will really be 3-tuples (K_i, A_i, B_i) where B_i is the address in the file of the record with key K_i. This address would consist of the cylinder and surface numbers of the track to be accessed to retrieve this record (for some disks this address may also include the sector number). The A_i, $0 \le i \le n$ are the addresses of root nodes of subtrees. Since these nodes are also on a disk, the A_i are cylinder and surface numbers.

```
   procedure MSEARCH(T,X)
   //Search the m-way search tree T residing on disk for the key
     value X. Individual node format is n,A_0,(K_1,A_1), ...,(K_n,A_n),
     n < m. A triple (P,i,j) is returned. j = 1 implies X is found
     at node P, key K_i. Else j = 0 and P is the node into which
     X can be inserted//
1    P <- T; K_0 <- [-∞]; Q <- 0          //Q is the parent of P//
2    while P ≠ 0 do
3      input node P from disk
4      Let P define n, A_0, (K_1,A_1), ..., (K_n,A_n)
5      K_{n+1} <- [+∞]
6      Let i be such that K_i ≤ X < K_{i+1}
7      if X = K_i then [//X has been found// return (P,i,1)]
8      Q <- P; P <- A_i
9    end
     //X not in T; return node into which insertion can take place//
10   return (Q,i,0)
11 end MSEARCH
```

Analyzing algorithm MSEARCH is fairly straightforward. The maximum number of disk accesses made is equal to the height of the tree T. Since individual disk accesses are very expensive relative to the time needed to process a node (i.e. determine the next node to access, lines 4–8) we are concerned with minimizing the number of accesses needed to carry out a search. This is equivalent to minimizing the height of the search tree. In a tree of degree m and height $h \geq 1$ the maximum number of nodes is $\sum_{0 \leq i \leq h-1} m^i = (m^h - 1)/(m - 1)$. Since each node has at most $m - 1$ keys, the maximum number of entries in an m-way tree index of height h would be $m^h - 1$. For a binary tree with $h = 3$ this figure is 7. For a 200-way tree with $h = 3$ we have $m^h - 1 = 8 \times 10^6 - 1$.

Clearly, the potentials of high order search trees are much greater than those of low order search trees. To achieve a performance close to that of the best m-way search trees for a given number of entries n, it is necessary that the search tree be balanced. The particular variety of balanced m-way search trees we shall consider here is known as a B-tree. In defining a B-tree it is convenient to reintroduce the concept of failure nodes as used for optimal binary search trees in §9.1. A failure node represents a node which can be reached during a search only if the value X being searched for is not in the tree. Every subtree with root $= 0$ is a point that is reached during the search iff X is not in the tree. For convenience, these empty subtrees will be replaced by hypothetical nodes called failure nodes. These nodes will be drawn square and marked with an F. The actual tree structure does not contain any such nodes but only the value 0 where such a node occurs. Figure 10.11 shows the 3-way search tree of figure 10.9 with failure nodes. Failure nodes are the only nodes that have no children.

Definition: A B-tree, T, of order m is an m-way search tree that is either empty or is of height ≥ 1 and satisfies the following properties:

(i) the root node has at least 2 children

(ii) all nodes other than the root node and failure nodes have at least $\lceil m/2 \rceil$ children

(iii) all failure nodes are at the same level.

The 3-way search tree of figure 10.11 is not a B-tree since it has failure nodes at levels 3 and 4. This violates requirement (iii). One possible B-tree of order 3 for the data of figure 10.9 is shown in figure 10.12. Notice that all nonfailure nodes are either of degree 2 or 3. In fact, for a B-tree of order 3, requirements (i), (ii) and the definition

balanced m-way search tree that permits search, insert, delete in $O(\log_m n)$ time